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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,054	09/15/2000	Randy M. Bonella	10559/350001/P10068	4989

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EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	8

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/662,054	Applicant(s) BONELLA ET AL.	
	Examiner Dennis M. Butler	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,8,9,11-13,16-25,27-42 and 45-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13 and 16-21* is/are allowed.

6)☒ Claim(s) *1-4,8,9,11,12,22-25,27-42 and 45-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to amendment A received on December 4, 2003. Claims 1-4, 8-9, 11-13, 16-25, 27-42 and 45-47 are pending. Claims 5-7, 10, 14-15, 26, 43 and 44 have been canceled. Claims 46 and 47 have been added.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. Claims 12, 22-25, 27-32, 36 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 12 and 28-32 are indefinite because they depend from canceled claims.

Regarding claim 22, the phrase "said non volatile memory" lacks proper antecedent basis. In addition, the relationship between the programmably delaying element and the determining element is unclear. The relationship between the pre-stored values and the delay values is unclear and it is unclear whether the pre-stored values are stored in the non volatile memory or some other memory.

Claims 23-25 and 27-32 are rejected because they incorporate the deficiencies of claim 22.

Regarding claim 36, the phrase "said location" lacks proper antecedent basis.

Regarding claim 38, the phrase "said using comprises" lacks proper antecedent basis. In addition, the claim is indefinite as to when the step is performed because there are two "using" steps in claim 37. One using step is performed when a system event is not detected and the other using step is performed only when the system event is detected.

4. Claims 1-4, 9, 22-23, 25, 33, 35, 37-39, 42 and 45-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Coteus et al., U. S. Patent 6,292,903.

Per claims 1-4, 9, 22-23, 25, 33, 35, 37-39, 42 and 45-46:

Coteus et al teach the claimed items including a data source having a plurality of different lines (Memory Controller 1 and/or DIMMs 14a-14n, Data In lines 104a-n and Data lines 105a-n of figures 2a and 2b), a plurality of programmable delay elements each coupled to one of the lines (Flip-Flops 10a2a-10a2n, Flip-Flops 10a3a-1-a3n and Delays 15a-15n and 16a-16n of figures 2A and 2B and figure 9a), storing values for the programmable delay elements in a register (Memory 3 of figure 1 and Delay Value Info of figure 2b), determining if a system event has occurred (system power-up of figure 3a), arbitration logic having first and second elements (microprocessor 2 and the operating program in memory 3) and testing the signals for the proper delay values (figures 3a-3f) at column 6, line 33 – column 8, line 30, at column 10, lines 10-16, at column 24, line 66 – column 25, line 10 and at column 25, line 65 – column 26, line 8.

5. Claims 8, 24 and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al., U. S. Patent 6,292,903 in view of Huang et al., U.S. Patent 6,041,419.

Per claims 8, 24 and 34:

Coteus does not explicitly describe that the signals are from a graphics device as claimed. However, Huang describes that it is known in the graphics processing art that graphics devices transmit signals that require synchronization by using programmable delay devices in order to properly sample the signals with figures

1 and 6, at column 1, lines 12-46 and at column 3, line 21 – column 4, line 14. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Coteus's smart memory interface in a graphics processing system in order to align the clock and data signals transmitted in the graphics processing system for proper sampling of the data signals. One of ordinary skill in the art would have been motivated to combine Coteus and Huang because of Coteus's suggestion of synchronizing signals in memory subsystems at column 1, line 65 – column 2, line 26. It would have been obvious for one of ordinary skill in the art to combine Coteus and Huang because they are both directed to the problem of synchronizing data and clock signals in memory subsystems.

6. Claims 11, 36, 40, 41 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al., U. S. Patent 6,292,903 in view of Jeddeloh, U.S. Patent 6,629,222.

Per claim 11:

Jeddeloh describes that it is known to store a delay value that produces a best desired result that is one where a plurality of delayed signals are received at substantially the same time with figures 4 and 6, at column 6, lines 9-16 and at column 7, lines 5-23. It would have been obvious to one having ordinary skill in the art at the time the invention was made to store a delay value that produces a best desired result in order to determine the best desired result delay value directly without performing a calculation. One of ordinary skill in the art would

have been motivated to combine Coteus and Jeddeloh because of Coteus's suggestion of synchronizing signals in memory subsystems at column 1, line 65 – column 2, line 26. It would have been obvious for one of ordinary skill in the art to combine Coteus and Jeddeloh because they are both directed to the problem of synchronizing data and clock signals in memory subsystems.

Per claims 40, 41 and 47:

Coteus does not explicitly describe the system event including a system component change or an operating system crash. However, Coteus describes the system event including a power up initialization event with figure 3a. It is well known to re-power and initialize the system when either a system component change or an operating system crash occurs. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to cause the system to be re-powered and initialized when either a system component change or an operating system crash occurs in order to recognize and initialize the component change, re-install the operating system and redetermine and reprogram the delay value in the programmable delay.

Per claim 36:

Coteus describes programmably delaying signals such that the signals are latched or loaded into a flip flop during an enablement period during a positive edge of a clock signal at column 6, lines 33-67. It would have been obvious to one having ordinary skill in the art at the time the invention was made to delay

signals such that they a skewed relative to a clock margin of a system in order to reliably latch or load the signals into flip flops using the clock.

7. Claims 13 and 16-21 are allowable over the art of record because the art of records corresponding arbitration logic determines the relative delay of outputs each time the system is powered up while the invention of claim 13 provides arbitration logic that determines the relative delay of outputs and is only responsive to a system event flag. The claimed arbitration logic determines the relative delay of outputs only after determining whether the system event flag indicates it is proper to do so.

8. Applicant's arguments filed on December 4, 2003 have been fully considered but they are not persuasive.

In the Remarks, applicant has argued in substance that:

A. The specific technique of storing sets of values and using the one that produces the best result is in no way taught or suggested by Coteus, Barth and/or Ohno no matter how combined.

B. The features of claim 1 of storing and testing different sets of delay values and obtaining the set that works best as the optimum delay set is not taught or suggested by the cited prior art.

C. The cited prior art does not teach or suggest an event detector and determining new delay values only when a specific event occurs.

D. The prior art does not teach or suggest that the delay values cause the signal to have a specified relationship with one another where the specified relationship is not synchronized.

9. As to point A, the examiner disagrees with applicant's contention. Coteus clearly describes storing the set of values that produces the best result as described in the above rejection. Figures 3e and 3f show values that produce the best result being stored as flag 16a1 and/or 16a2. In addition, claim 1 does not recite using the one that produces the best result. The claim stops at storing the result. Therefore, it is irrelevant whether Coteus teaches this feature.

As to point B, claim 1 does not recite storing different sets of values that are tested. Claim 1 recites that a first element produces a set of first values. Therefore, it is irrelevant whether Coteus teaches storing sets of values and testing each set of values. Claim 1 does not recite obtaining the set that works best as the optimum delay set. Claim 1 merely recites storing the plurality of values that produce a best desired result. Therefore, it is irrelevant whether Coteus teaches this feature.

As to point C, the examiner disagrees with applicant's contentions. As described in the above rejections, Coteus describes determining if a (specific) system event has occurred with detecting or determining the system power-up of figure 3a, at column 10, lines 10-21 and at column 24, line 66 – column 25, line 10. Coteus clearly describes an event detector (microprocessor 2) and determining new delay values only when a system event (power up) occurs (figure 3).

As to point D, the examiner disagrees with applicant's contention. Claim 42 recites the programmable delay controls the signals to have a specified relationship with one another at said at least one specified location where the specified relationship is not synchronized. If the signals were synchronized at each location, the programmable

delay would not be needed because the signals would always remain synchronized. Coteus describes programming different values into a plurality of programmable delays in order to compensate for the different lengths and speed of busses coupling memory modules at column 1, line 65 – column 2, line 26 and at column 2, line 64 – column 3, line 10. A signal that travels over a longer line must be faster that a signal traveling over a shorter line in order for them to arrive at the input device at substantially the same time. Therefore, the fast and slower signals are not synchronized at each location. They are synchronized only at the input device location. Coteus does not describe that each signal is synchronized at each point along the signal path as implied by applicant. The signals programmably delayed by Coteus are clearly not synchronized at at least one specified location and Coteus teaches the invention to the extent claimed.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Dennis M. Butler
Primary Examiner
Art Unit 2115